## REMARKS

Favorable reconsideration of this application is respectfully requested in view of the claim amendments and following remarks. By virtue of the amendments, Claims 1-5 and 7-23 are pending in the present application of which Claims 1, 9 and 19 are independent. Claims 1, 9, and 19 have been amended for clarity. No new matter has been added.

Claims 1, 9 and 19 were rejected under 35 U.S.C. § 102(b) as being anticipated by Jim Handy, Cache Memory, 2nd edition ("Handy"). Claims 2-5, 7-8, 10-18 and 20-23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Handy in view of U.S. Patent No. 6,209,065 to Van Doren et al. ("Van Doren et al.") These rejections are respectfully traversed for at least the reasons set forth below.

*Examiner Interview*

Examiners Jasmine Song and Kevin Verbrugge are thanked for the courtesies extended during the personal interview with the undersigned and Paramita Ghosh on June 3, 2004.

*Claim Rejection under 35 U.S.C. § 102*

The Official action sets forth a rejection of Claims 1, 19 and 19 under 35 USC 102 (b) as being allegedly anticipated by Handy. This rejection is respectfully traversed.

Handy does not anticipate the subject matter of independent Claims 1, 9 and 19. Specifically, Handy does not disclose the step of "in the processor having the valid copy of the data, returning the valid copy of the requested data to the requesting processor," as recited in Claim 1.

In the pages cited by the Examiner, Handy discloses the MESI protocol. (p. 156) Table 4.1 on p. 157 "shows the four MESI states and the responses given in the event of processor and snoop read and write hits and misses in cacheable spaces." (p. 157) The protocol described on pp. 157-158 does not disclose a processor "returning the valid copy of the requested data to the requesting processor," as recited in Claim 1. Handy discloses that, for the MESI protocol, "there is no . . . direct data intervention." (pp. 156, last line -157, line 1) Handy's glossary defines direct data intervention as "a bus cycle in a multiple-processor system during which one processor's bus read is satisfied by data supplied from another processor's cache." (p. 206) Thus, Handy does not disclose a processor having valid data returning the valid data to the requesting processor.

Handy further does not disclose that "one of said two or more processors that modified the data is configured to return the valid copy of the modified data to the one of the two or more processors or memory that issued the request," as recited in Claims 9 and 19. As discussed above with respect to Claim 1, Handy does not disclose a processor configured to return the valid data to a processor that issued a request.

Further, Handy does not disclose "from a requesting processor, issuing a request for the modified data to one or more other processors and memory," as recited in Claim 1, "each of the two or more processors being in communication with the memory controller for issuing a request for the modified data to the others of the two or more processors and said memory," as recited in Claim 9, or "each of the two or more processors being operable to issue a request for the modified data to the others of the two or more processors and said memory," as recited in Claim 19. As discussed above, since the MESI protocol described in Handy does

not have direct data intervention, Handy does not disclose a requesting processor issuing a request for the modified data to one or more other processors.

Handy also does not disclose "two or more processors, each in communication with a shared memory via a memory controller," as recited in Claim 9. There is no mention of a memory controller in the passages recited by the Examiner. Therefore, Claims 1, 9 and 19 are allowable over Handy.

*Claim Rejection Under 35 U.S.C. §103*

The test for determining if a claim is rendered obvious by one or more references for purposes of a rejection under 35 U.S.C. § 103 is set forth in MPEP § 706.02(j):

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck,* 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Therefore, if the above-identified criteria are not met, then the cited reference(s) fails to render obvious the claimed invention and, thus, the claimed invention is distinguishable over the cited reference(s).

The Official Action sets forth a rejection of Claims 2-5, 7-8, 10-18 and 20-23 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Handy in view of Van Doren et al. This rejection is respectfully traversed.

As described above, Handy does not disclose or teach all of the elements of independent Claims 1, 9 and 19. Van Doren et al. discloses "a mechanism for reducing the

latency of inter-reference ordering between sets of memory reference operations in a distributed shared memory multiprocessor system including a plurality of symmetric multiprocessor (SMP) nodes interconnected by a hierarchical switch." (Col. 3, lines 47-52) Van Doren et al. discloses that "when a processor P issues a request to the system, the system one or more probes . . . to other processors." (Col. 7, lines 3-5) A "coherence controller generates the necessary probes (e.g., a Fill x and Inval x) and forwards them to the output queues 226 and 228 for transmission to the processors." (Col.7, lines 59-62) "Each time a probe-type command is sent to the global port, an entry is created in the LoopComSig table; when a corresponding probe-ack returns to the node's Arb bus, the entry is cleared." (Col. 11, lines 58-62) Thus, since the processors in Van Doren et al.'s system receive probes that require acknowledgement generated by a coherence controller, the processors do not determine if the data in their caches are valid or invalid, and the processors do not drop the request without responding to the request. Therefore, Van Doren et al. does not disclose the steps of "in each of the processors and memory that receive the request, checking to determine whether a stored copy of the data is valid or invalid" and "in the processors and memory that have invalid copies of the data, dropping the request without responding to the request" as recited in independent Claim 1.

Similarly, Van Doren et al. does not disclose "when one of the two or more processors issues a request for the modified data, each of the two or more processors and the shared memory that receives the request being operable to check itself to determine whether a stored copy of the data is valid or invalid" and "wherein the one of said two or more processors that modified the data is configured to respond to the request, and the processors

and memory having invalid copies of the data are configured to drop the request without responding to the request," as recited in Claims 9 and 19.

Thus, Van Doren et al. does not teach or suggest the invention of independent Claims 1, 9 and 19. Further, it would not have been obvious to one of ordinary skill at the time of the invention set forth in Claims 1, 9 and 19 to combine the teachings of Handy and Van Doren et al. In the MESI protocol set forth in Handy, "there is no . . . direct data intervention" (pp. 156, last line -157, line 1), as discussed above.

Further, since Handy does not teach a requesting processor issuing a request for the modified data to one or more other processors, Handy also does not teach "in each of the processors and memory that receive the request, checking to determine whether a stored copy of the data is valid or invalid" and "in the processors and memory that have invalid copies of the data, dropping the request without responding to the request" as recited in independent Claim 1. Similarly, Handy does not teach "when one of the two or more processors issues a request for the modified data, each of the two or more processors and the shared memory that receives the request being operable to check itself to determine whether a stored copy of the data is valid or invalid" and "wherein the one of said two or more processors that modified the data is configured to respond to the request, and the processors and memory having invalid copies of the data are configured to drop the request without responding to the request," as recited in Claims 9 and 19. Thus, the combination of Handy and Van Doren et al. would not have resulted in the invention as claimed in Claims 1, 9 and 19.

Thus, independent Claims 1, 9 and 19, and their dependent Claims 2-5, 7-8, 10-18 and 20-23 are allowable over any proposed combination of Handy and Van Doren et al.

The Official Action asserts that Van Doren et al. discloses features of dependent Claims 2-5, 7-8, 10-18 and 20-23. Although Applicant disagrees with this characterization of the features of dependent Claims 2-5, 7-8, 10-18 and 20-23, Applicant reserves the right to pursue such arguments at a later date.

*Conclusion*

In light of the foregoing, withdrawal of the rejections of record and allowance of this application are earnestly solicited.

Should the Examiner believe that a further telephone conference with the undersigned would assist in resolving any issues pertaining to the allowability of the above-identified application, please contact the undersigned at the telephone number listed below. Please grant any required extensions of time and charge any fees due in connection with this request to deposit account no. 08-2025.

Respectfully submitted,

Fong Pong

Dated: June 10, 2004 By

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